

**KUMAR ABHINAV RAJPUT**  
**HOUSE NO. C-205, PANDAV NAGAR**  
**AKSHARDHAM, NEW DELHI**  
**DELHI-110092 (INDIA)**  
**Mob No: +91-8527333171, 9457425966**  
**Email: [kumar.abhinav792@gmail.com](mailto:kumar.abhinav792@gmail.com)**



## EDUCATION

Year	Degree/Certificate	University/School	CGPA/Score
2016	Dual Degree B.Tech+M.Tech (VLSI) Electronics & Communication Engineering	Gautam Buddha University Greater Noida(UP)	7.81
2010	XII (UP Board)	S.V.M. Inter College, Dhampur	79.0%
2008	X (UP Board)	S.V.M. Inter College, Dhampur	68.0%

## TRAINING AND PROJECTS

### Verilog HDL Training Coursework

*[Jun'15-Jul'15]*

- Completed 6 Weeks certification course in Verilog HDL at DUCAT-Greater Noida.
- Gained more knowledge of programming with the help of Logic Design Concepts.

### Room Appliances Controller- B.Tech Project

*[Feb'15-May'15]*

- B.Tech project on automatic room appliances controller using 8051 microcontroller and visitor counter.
- This project was very useful for such problems as one generally forgets to turn off lights and fans while leaving a room.
- Major responsibility of **hardware design and programming in embedded C**.

### Elevator Controller using Verilog HDL- B.Tech Project

*[Aug'15-Dec'15]*

- B.Tech project on Elevator Controller using Verilog HDL Programming.
- The aim of project was to control lift motion, indicate direction of motion, and present floor level.

### Design SRAM Cell- M.Tech Project

*[Jan'16-May'16]*

- M.Tech project on **Reduce leakage power of SRAM Cell** Using Forced Sleep and Variable Body Biasing Technique in submicron technology.
- The main motivation of the project was reduce leakage power of SRAM cell and maintain the exact logic state in sleep mode.

**Design Hybrid Full Adder- M.Tech Project**

[Jan'16-May'16]

- M.Tech project on parametric analysis of power and delay of **1 bit Full Adder using hybrid CMOS** in submicron technology.
- Idea behind the project was to achieve good-drivability, noise-robustness, and low-energy operations for deep sub micrometer technology.

**RELEVANT COURSEWORK/SKILLS/EXPERIENCE**

Coursework	Semiconductor Theory   Analog& Digital Electronics   Communication Systems Control System   CMOS Design   Microprocessor   Optical Communication
Language & Software	C Programming   C++ Programming   Core JAVA   Verilog HDL Modalism   Cadence Virtuoso   AutoCAD
Operating System	Windows   Red Hat Linux

**ACHIEVEMENT/CURRICULAR ACTIVITIES/HOBBIES**

Academics	<b>Department Rank 5<sup>th</sup></b> among a class of more than 45 students.
Cultural activity	Coordinator of Abhivyanjana Techno culture 2014, the annual tech fest of GBU.
Workshops	Attend a workshop organized by DKOB Lab Noida for <b>Verilog and FPGA</b> . Attend a workshop organized by RADDIANCE EDUTECH for <b>analog circuit design</b> .
Achievement & Publication	Qualified <b>GATE Exam-2016</b> .  Kumar Abhinav, R.B. Singh " <b>Reduce Leakage Power of SRAM Cell using Variable Body Biasing and Force Sleep Technique in Submicron Technology</b> ", International journal of computer networks and wireless communications ( <b>IJCNWC</b> ) Vol.6, No 3, May-June 2016.
Strength & Hobbies	Self-motivated, initiative, creative, high level of energy. Cricket, Badminton and Listing music.

I hereby certify that the information given above is true and correct to the best of my knowledge and belief.

Kumar Abhinav Rajput